REMARKS

Claims 1-4, 6-9, 11-13, 16-17, 19-32, 34-35, 38, 40-41, 44, 47, 50, 52-53, 56, and 58-64 are pending in this application. Claim 46, which recites the same subject matter as claim 22, has been canceled without prejudice or disclaimer. Claims 1 and 11 have been amended without introduction of new matter. Favorable reconsideration is respectfully requested in view of the above amendments and the remarks advanced below.

The undersigned notes with appreciation the courtesies extended by Examiner Vicary during a telephonic interview conducted on February 4, 2010. Page 4 of the Interview Summary issued by the Examiner on February 17, 2010, correctly captures the substance of that interview. As noted in that Interview Summary, paragraph 49 of a final rejection issued in a related, Application No. 11/752,300, identifies subject matter that the Examiner considers allowable if added to independent claim 1. The reference to "Figure 2" in that Interview Summary concerns a discussion between the undersigned and the Examiner of the following statement from paragraph 49 of the final action in the related application: "Other possible subject matter includes … explicitly conveying the concept that the instant invention's processing element can *store* a variable amount of data (e.g., Figure 2), as opposed to Clauberg in which each processing element must store an entire fixed-length cell." (See, Application No. 11/752,300, paragraph 49 of the final Office Action dated December 21, 2009.) In view of this indication of allowable subject matter, claim 1 is amended to include the concept that the claimed processing element is operable to store and process a variable amounts, or different amounts of data.

Claims 1-4, 6-9, 11, 16-17, 20, 21, 32, 40, 44, 52, 56, 59, 60, 63 and 64 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over the Marsan et al. paper "Router Architectures Exploiting Input-Queued, Cell-Based Switching Fabrics" in view of Clauberg (WO 97/29613). However, independent claim 1 is amended to include subject matter that the Examiner indicated as allowable. Hence, it is believed the rejection of claim 1 is overcome.

Dependent claims 2-4, 6-9, 11, 16-17, 20, 21, 32, 40, 44, 52, 56, 59, 60, 63 and 64 also are believed allowable because they each depend either directly or indirectly from allowable claim 1.

The remaining dependent claims are rejected under Section 103(a) using the Marsan et al. paper and the Clauberg document as applied to claim 1 together with various combinations of the Kejriwal et al patent (U.S. Patent No. 6,704,794) and ISSC95 (Evening Discussion Session). However, neither the Kejriwal et al patent nor the ISSC95 document

remedy the shortcomings of the Marsan et al. paper and the Clauberg document with respect to the presently claimed combination of features.

The final Office Action also includes a rejection under 35 U.S.C. § 112, second paragraph, of claims 1-4, 6-9, 11-13, 16-17, 19-22, 32, 34, 35, 38, 40, 41, 44, 46, 47, 50, 52, 53, 56 and 59-64 as allegedly being indefinite. Applicant requests withdrawal of this rejection for the following reasons:

With respect to claim 1, in section 6 of the Action, the Examiner objected to the term "in batches" because it is allegedly unclear "whether batches in the claim refers to the data packets, or that which the data packets are distributed into." While it is believed that those of ordinary skill in the art would understand, at least from the passages of the specification cited in the first paragraph of page 16 of the June 25, 2009, Amendment to support this feature, claim 1 had been changed to insert "batches of" before "data packets" to make it abundantly clear that "batches" refers to the recited data packets. Claims 2-4, 6-9, 11-13, 16, 17, 19-22, 32, 34, 35, 38, 40,41, 44, 46, 47, 50, 52, 53, 56 and 59-64, each of which depends either directly or indirectly from claim 1, have therefore similarly been clarified.

With respect to claim 7, in section 7 on page 3 of the Action, the Examiner again objected to the limitation "the processing elements are operable to control the input device" for the reason that "it appears that it is not the processing elements which control the input device, but the thread sequence controller." However, it is to be initially noted that Applicant amended claim 7 in the Amendment dated June 25, 2009, to recite that "the processing elements are operable to control the transfer of packet portions to the processing elements from the input device." In section 47, starting on page 17, the Examiner states the following: "while data transfer may be controlled by the processor, as claimed in claim 7, the claim mandates that data transfer is controlled by the *processing elements.* See Figure 4, which shows the processing elements as merely a part of the overall processor; the thread sequence controller, for example, is part of the processor but not the processor elements." It appears from these statements that the Examiner queries the point of control within the claimed invention. In reply, Applicant provides the following:

In a parallel processing implementation, control is distributed by design. Through the division, distribution and co-ordination of work, the workload is distributed across the design. This distribution of workload is carefully architected to avoid the creation of bottlenecks or pinch-points to achieve a more robust implementation that delivers high levels of processing

performance despite traffic load variation. To effectively distribute work without incurring bottlenecks, control is distributed.

The disclosed embodiment shows the use of multiple MTAP blocks (e.g., see Figure 6 and Figure 9) also referred to as MTAP processors. The structure of the MTAP unit is taught in Figure 4. An MTAP comprises a Thread Sequence Controller (TSC), Processing Element and I/O Engine. The TSC coordinates the plurality of processing elements as they process the work that is distributed to them. The TSC coordinates the status of the PEs with external status information and selects which of the available instruction streams to provide instructions streams from, in order to ensure the PEs are productively occupied.

Each PE operates on the same instruction but processes its own data. The TSC broadcasts an instruction across the plurality of PEs. The instruction broadcast is the next instruction for execution from the selected instruction stream; the instruction stream being chosen, from the available streams, for execution partly in dependence upon the PEs' collective state.

As the PEs execute, the selected instruction stream may be switched, for example if an instruction stream is blocked due to resource contention. The selection of which instruction stream to execute is based on a number of factors, including the collective status of the PEs and that of the wider system.

The software programmer controls the number, content and coordination of the instruction streams. This defines how the system will operate. The TSC coordinates which stream is to be executed and the delivery of instructions to the PEs.

Even though all PEs receive the same instruction stream, in the case of conditional statement execution, some PEs will execute one branch of the conditional statement and other PEs will execute the other branch. In this way, the individual state of each PE is data-dependent and is independent from that of other PEs in the array. The PEs then are more than a simple array of fixed function units (as may be the case in a VLIW implementation); each must maintain their own state information as they execute the instruction they receive.

The PEs are instrumental in the execution flow of the overall system; and the PEs do require the coordination and instruction stream management provided by the thread sequence controller. The combination of a processing array with the thread-sequence controller forms a multi-threaded SIMD array processor. Multiple MTAP processors can be instantiated to form the preferred embodiment of the instant application.

It is by the PEs executing an instruction stream that a data packet request will be made by the MTAP. The packet request instructions will form one of the instruction streams available for selection (and execution by the TSC). Thus, the PEs are operable to control the transfer of packet portions to the PEs for the input device, as set forth in claim 7. For these reasons, it is believed one of ordinary skill in the art would understand and find clear the recited features relating to PE control transfer of packet portions in claim 7. Claim 8, which depends from claim 7, is believed clear for the same reasons given above.

With respect to claim 9, in section 8 on pages 3 and 4 of the Action, the Examiner again objected to the limitation "the processing elements are operable to control an output device" for the reason that "it appears that it is not the processing elements which control the output device, but the thread sequence controller." However, Applicant notes that claim 9 was amended in the Amendment dated June 25, 2009, to recite that "the processing elements are operable to control the transfer of packet portions from the processing elements to an output device." Also, in a manner analogous with the above explanation of PE control of transfer of packets portions from an input device to PE, it is also by the PEs executing an instruction stream that a data packet output request will be made by the MTAP. Hence, the PEs are operative to control the transfer of packet portions from the PEs to an output device. For these reasons, it is believed the rejection of claim 9 under Section 112 should be withdrawn.

Finally, in section 9 on page 4 of the Action, the Examiner stated that "said input devices" and "said output devices" lack antecedent basis. While Applicant believes one of ordinary skill in the art would understand that these recitations are referring to the "input device" first recited in line 2 of claim 1, and the "output device " first recited in line 3 of claim 9, claim 11 has been changed to literally recite the singular form of the word "device." It is believed these amendments full address the Examiner's concerns with respect to proper antecedent basis.

The application is believed to be in condition for allowance. Prompt notice of same is respectfully requested.

Respectfully submitted,

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